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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
JONES, DAVID	
ART UNIT	**PAPER NUMBER**
2622	

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3

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/631,036	PEW ET AL.	
	Examiner	Art Unit	
	David L Jones	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 7/31/00 was filed after the mailing date of the application on 7/31/00. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Fig. 1, items #36, #38, #40, #42; Fig. 2, items #202 and #212. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3, 9-11, and 14-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Ambalavanar et al. U.S. Patent 5,579,452.

Regarding claim 1, Ambalavanar et al. discloses a printing system that comprises a first address bus (fig. 2, #28), a second bus (fig. 5, #72), and a bus gateway (fig. 2, #88) which functions as an address translation unit that provides seamless access between the Vbus and the Sbus, and decodes virtual addresses from bus masters (column 9, lines 45-61), i.e. transfer modules (fig. 2, #36A-#36E). Further, Ambalavanar et al. teaches (column 10, lines 31-45) that transfer modules #36A-#36E (which includes a packet buffer, **bus interface or bus master**, and a DMA Transfer Unit) are connected so that any of them can be used to transfer information to physical memory, hard drive #34 and EPC memory #24.

Regarding claim 2, Ambalavanar et al. teaches that bus gateway #88 provides interface between the Sbus and the Vbus. Further, it provides address translation for access to address spaces in then Vbus real address range, and passes a virtual address to the Sbus for virtual addresses in the Sbus range (column 9, lines 45-61). And it would be inherent that as is disclosed in column 10, lines 12-30, that to allow for storage in memory #74 of the Sbus that bus gateway #88 would be able to transmit to physical address on the Sbus.

Regarding claim 3, Ambalavanar et al. teaches that in figure 2, that the transfer module #36D of the Vbus is connected to decomposer #64, which in turn is connected to the IOT, which as defined by Ambalavanar et al. (column 6, lines 26-32) image output terminal that includes a xerographic print engine.

Regarding claim 9, Ambalavanar et al. discloses a plurality of transfer modules (#36A-#36E), each consists of DMA Transfer Units, which act like DMA controllers that control all memory access along with the bus interface. Although, Ambalavanar et al. does not explicitly disclose that the transfer modules map the virtual address, but it is implied, since that the gateway receives and decodes virtual addresses from the transfer modules (column 9, lines 54-59), and by definition it has to generate the virtual address for mapping. Further, the CPU accordingly generates both virtual and physical addresses mapping by inclusion of a resource manager fig. 9, #300. Further, a bus gateway (fig. 2, #88), which functions as an address translation unit that provides seamless access between the Vbus and the Sbus, and decodes virtual addresses from bus masters, i.e. transfer modules (fig. 2, #36A-#36E) and the controller #44.

Regarding claim 10, Ambalavanar et al. discloses a plurality of memory #24, #34, and #76 coupled to the gateway #88.

Regarding claim 11, Ambalavanar et al. discloses that the gateway #88 provides address translation for access to address spaces in then Vbus real address range (column 9, lines 45-61) in memory #24 and #34.

Regarding claims 14 and 19, Ambalavanar et al. discloses a system that includes a CPU #44, a plurality of transfer modules #36A-#36E that include DMA controllers in each, and a plurality of memory #24, #34, #76. Further, Ambalavanar et al. discloses a gateway #88 that functions as an address translation unit (column 9, lines 45-61), and it would be inherent that a CPU #44 would be able to transmit a plurality of virtual addresses to the gateway for translation.

And Ambalavanar et al. discloses that the transfer modules transmit virtual addresses to the gateway (column 9, lines 45-61).

Regarding claims 15, 16, 17, 18, and 20, Ambalavanar et al. teaches that bus gateway #88 provides interface between the Sbus and the Vbus. Further, it provides address translation for access to address spaces in then Vbus real address range, and passes a virtual address to the Sbus for virtual addresses in the Sbus range (column 9, lines 45-61). And it would be inherent that the ATU is able to generate physical addresses from the virtual addresses to be sent by the CPU #44, since the gateway is able to decode virtual addresses from the transfer modules. The gateway also includes a DMA channel for memory-to-memory transfers, which would allow it to transmit the physical memory addresses of memory #24, #34, or #76.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ambalavanar et al. as applied to claims 1-3, 9-11, and 14-20 above, and further in view of Kawai et al. U.S. Patent 5,355,441.

Regarding claim 4, Ambalavanar et al. discloses a controller that is a SPARC processor manufactured by SUN MICROSYSTEMS, INC that is coupled to the Sbus. Whereas, Kawai et al. discloses a first CPU (fig. 2, #305) that is connected to the first bus #313, and a second CPU

#310 connected to the second bus #312. Therefore, it would have been obvious to one skilled in the art at the time the invention was made to include a processor on both buses to further speed up the system and by using a second CPU on the first bus of Ambalavanar et al. application it will allow for faster interpretation of print data commands.

Regarding claim 5, Ambalavanar et al. discloses a plurality of bus transfer modules (#36A-#36E) coupled to the Vbus, each consists of DMA Transfer Units, which act like DMA controllers.

Regarding claim 6, Ambalavanar et al. discloses a hard disk memory (fig. 5, #76) connected to the Sbus.

Regarding claim 7, Ambalavanar et al. teaches that bus gateway #88 provides interface between the Sbus and the Vbus. Further, it provides address translation for access to address spaces in then Vbus real address range, and passes a virtual address to the Sbus for virtual addresses in the Sbus range (column 9, lines 45-61). Although, it is not explicitly disclosed that the CPU disclosed by Kawai et al. and the Vbus arbiter taught by Ambalavanar et al. would be able transmit virtual addresses to the ATU on the Vbus, but it would be inherent that the CPU and Vbus arbiter are both operable to transmit virtual addresses to the ATU on the Vbus thereby allowing access to all virtual addresses.

Regarding claim 8, Ambalavanar et al. teaches that bus gateway #88 provides interface between the Sbus and the Vbus. Further, it provides address translation for access to address spaces in then Vbus real address range, and passes a virtual address to the Sbus for virtual addresses in the Sbus range (column 9, lines 45-61). And it would be inherent that as is disclosed in column 10, lines 12-30, that to allow for storage in memory #74 of the Sbus that bus gateway

#88 would be able to transmit to physical address on the Sbus, thereby allowing the CPU disclosed by Kawai et al. and the Vbus arbiter taught by Ambalavanar et al. to address physical memory addresses on the Sbus through translation by the gateway from virtual addresses to physical addresses.

7. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ambalavanar et al. and Kawai et al. as applied to claims 1-11, and 14-20 above, and further in view of McCarthy et al. U.S. Patent 5,029,070.

Regarding claim 12, Ambalavanar et al. and Kawai et al. disclose two address buses. Ambalavanar et al. discloses and a controller #44, but they do not detail between a physical bus and a virtual bus. Whereas, McCarthy et al. discloses a physical address bus (fig. 2, #45), virtual memory bus (fig. 2, #35), a CPU coupled to the virtual memory bus, and I/O controller #10 connected to both the virtual memory and the physical memory. The I/O controller performs the same similar functions of a DMA controller as disclosed in column 8, lines 4-11. And a global memory (fig. 4, #13) is attached to physical address bus #6. Therefore, it would have been obvious to one skilled in the art at the time the invention was made that to detail the address buses as taught McCarthy et al. in the application by Ambalavanar et al. to allow for a more streamlined pipeline of data. Further, it follows that the Vbus is a Virtual Bus and the Sbus is a physical bus.

Regarding claim 13, Ambalavanar et al. teaches that in figure 2, that the transfer module #36D of the Vbus is connected to decomposer #64, which in turn is connected to the IOT, which

as defined by Ambalavanar et al. (column 6, lines 26-32) image output terminal that includes a xerographic print engine.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Askinazi et al. U.S. Patent 4,453,211discloses a single synchronous system bus interconnecting a number of distributed processors, which emulate multiple channels of a multi-channel system. Young et al. U.S. Patent 4,694,395 discloses a system is disclosed which reduces the cycle time required for performing virtual look-ahead memory operations in computer systems employing random access memory and paging. Beck et al. U.S. Patent 5,146,547 discloses a page printer which rasterizes a page utilizing partial page bit map swaths.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David L Jones whose telephone number is (703) 305-4675. The examiner can normally be reached on Monday - Friday (7:00am - 3:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Coles can be reached on (703) 305-4712. The fax phone number for the organization where this application or proceeding is assigned is (703)-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4750.

David L. Jones

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